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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,074	10/20/2005	Siegfried Mantl	23391	2822

535 7590 09/15/2008

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ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
09/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,074	MANTL, SIEGFRIED	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-22,24-28,32,35-37,39,42,43,45,48,50-79,97 and 98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5,10-22,24-28,32,35-37,39,42,43,45,48,50-79,97 and 98* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/2/07.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 54-55,60-61,68-70,73, and 77-78 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Regarding claims 54-55, "the layer structure" and "the applied layers" lack antecedent basis. The meaning of "noticeable relaxation" is not clear. Since the size of invention disclosed in the specification is in the nanometer range, even one with good eyesight might not notice any changes in the device.

4. Regarding claims 60-61, the thicknesses of the second layer claimed are negative values.

5. Regarding claims 45, 68-70 and 73, "the layers" claimed in claims 68 and 73 lack antecedent basis.

6. Regarding claims 77-78, "the layer 3" claimed in claim 77 lacks antecedent basis.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3,10-21,25-28,32,35-37,39,42,45,50-56,60-64,66,71-72,74-79 are rejected under 35 U.S.C. 102(b) as being anticipated by Christiansen et al (PG Pub 2002/0185686 A1).

9. Regarding claim 1, 56, 71, 74-79, Christiansen teaches a method of producing a strained layer (SiGe layer 410 in fig. 13) on a substrate, the method comprising the steps of: providing at least one first epitaxial relaxing layer (SiGe layer 410 in fig. 13) on an SOI-substrate, producing a defect region (paragraph [0023]) in a layer (paragraph [0011], see layer 410 in fig. 13) neighboring a silicon layer (layer 50, paragraph [0003]) of the SOI-substrate to which strain is to be transferred, and relaxing at least one layer (layer 410) neighboring the silicon layer to strain the silicon layer of the SOI-substrate and to produce the strained silicon layer (layer 50); wherein a layer to be strained has a thickness d3 in the range of 1 to 50 nanometers (paragraph [0084]); further comprising the step of carrying out at least one further thermal treatment for relaxation of one or more layers (claims 39 and 44, relaxed layer SiGe); further comprising the step of producing on a strained region of the layer an n- and/or p- MOSFET (paragraph [0003]); further comprising the step of depositing a further epitaxial layer comprising silicon or silicon/germanium or an Si-Ge-C layer or a germanium layer (claim 26); further comprising the step of producing on a strained silicon-germanium region p- MOSFETs as further epitaxial layers or as nonrelaxed layers structures (paragraph [0003]); further comprising the step of producing on unstrained region of the layer 3 to be strained, bipolar transistors (paragraph [0003]); wherein for producing a bipolar transistor, a

silicon- germanium layer is applied (paragraph [0003]); wherein the steps of claim 1 are carried out a plurality of times (claim 26).

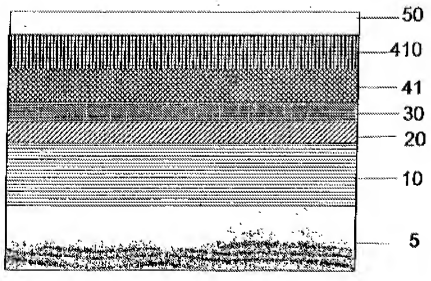


FIG 13

10. Regarding claim 2, Christiansen teaches the method according to claim 1, further comprising the step of forming defects (in layer 410 in fig. 13) that give rise to relaxation of at least one neighboring layer of the layer which is to be strained.

11. Regarding claim 3, Christiansen teaches the method according to claim 1, further comprising the step of subjecting the layer structure for relaxation to a thermal treatment and/or oxidation (paragraph [0061]).

12. Regarding claim 10, Christiansen teaches the method according to claim 1 wherein two neighboring layers of the layer to be strained have other degrees of stress

than the layer to be strained. Note that the two layers below Si strained layer each has different stress due to the weight of the layer(s) above.

13. Regarding claim 11, Christiansen teaches the method according to claim 1 wherein a plurality of layers are relaxed. Two sets of a fourth relaxed layers are formed (see claim 65).

14. Regarding claim 12, Christiansen teaches the method according to claim 1 wherein a plurality of layers (SeGe layers) to be strained, have strain transferred to them.

15. Regarding claim 13, Christiansen teaches the method according to claim 1, further comprising the step of depositing on the first layer epitaxially at least one second layer with a different lattice structure (the fourth layer, see claim 46).

16. Regarding claim 14, Christiansen teaches the method according to claim 13 wherein the defect region is produced in the second layer (threading disclocation, see claim 76).

17. Regarding claim 15, Christiansen teaches the method according to claim 1 wherein on the layer to which strain is to be transferred at least one graded layer is deposited as the first layer (SiGe layer, see paragraph [0003]).

18. Regarding claim 16, Christiansen teaches the method according to claim 15 wherein at the region of the layer to be strained, the graded layer (SiGe layer) has a degree of strain that is different from that of the layer (Si layer) to be strained. Note that the limitation in the claim is inherent that the graded layer has a different degree of

strain from that of the Si layer at least because of the weight exerted on the SiGe layer by the Si layer.

19. Regarding claim 17, Christiansen teaches the method according to claim 15, further comprising the step of producing a defect region (e.g. caused by He implants in the SiGe layer) in the graded layer.

20. Regarding claim 18, Christiansen teaches the method according to claim 1, further comprising the step of depositing an epitaxial layer (Si layer) structure comprising a plurality of layers (Si and SiGe) on the substrate.

21. Regarding claims 19-21 and 25, Christiansen teaches the method according to claim 1, further comprising the step of relaxing the first layer by a thermal treatment; wherein the thermal treatment is done at a temperature between 550 degrees and 1200 degrees C; wherein the thermal treatment is done at a temperature between 700 degrees and 980 degrees C; further comprising the step of applying a mask (see paragraphs [0061] and [0075]).

22. Regarding claims 26-28, 32, 36-37, and 39, Christiansen teaches the method according to claim 1 wherein the defect region is produced by ion implantation; wherein for the implantation, hydrogen ions or helium ions are used; wherein the hydrogen ions or helium ions are implanted with a dose of 3×10^{15} to 4×10^{16} cm^{-2} (paragraphs [0010] and [0061]); wherein at least two implantations are carried out (claims 17 and 20); further comprising out the step of carrying out two implantations to produce two defect regions in the first layer and in the second layer; wherein the substrate during the ion implantation is tilted at an angle greater than 7 degrees, wherein between two

implantations a thermal treatment is carried out (claim 26); wherein the defects are produced in a Si-C layer by thermal treatment (claims 46, 52, and part (f) of claim 29).

23. Regarding claim 35, Christiansen teaches the method according to claim 13, further comprising out the step of carrying out two implantations to produce two defect regions in the first layer and in the second layer (column 26).

24. Regarding claim 42, Christiansen teaches the method according to claim 1 wherein a silicon surface layer (layer 50 in fig. 13) of the SOI substrate (paragraph [0012]) is the layer to be strained and the SiO2 of the SOI substrate forms the insulator of the substrate.

25. Regarding claim 45, Christiansen teaches the method according to claim 1 wherein the layer (SiGe layer) neighboring the silicon layer becomes viscous (pseudomorphic, see paragraph [0066], for example) at a temperature required for the relaxation.

26. Regarding claim 50, Christiansen teaches the method according to claim 13 wherein silicon (layer 50 in fig. 13, see paragraph [0077]) as the material for the second layer (layer 410) which is deposited upon the first layer.

27. Regarding claim 51, Christiansen teaches the method according to claim 15, further comprising the step of selecting Si-Ge as the material for a graded layer (paragraph [0003]).

28. Regarding claim 52, Christiansen teaches the method according to claim 51 wherein the germanium concentration in the graded layer (layer 47, paragraph [0080])

decreases from the interface with the layer to be strained to the surface of the graded layer.

29. Regarding claim 53, Christiansen teaches the method according to claim 15 wherein the germanium concentration in a Si-Ge (layer 46) layer at the interface with the layer to be strained is 100 percent (paragraph [0079 where x=1).

30. Regarding claim 54 (as understood), Christiansen teaches the layer structure has thickness (paragraph [0004]).

31. Regarding claim 55, Christiansen teaches the method according to claim 54 wherein the dislocation density after the growth amounts to less than 10^5 cm^{-2} (paragraph [0014]).

32. Regarding claims 60-61, Christiansen teaches the second layer has thickness.

33. Regarding claim 62, Christiansen teaches the method according to claim 1 wherein the layer to be strained is locally strained (strain in the strained Si layer 50).

34. Regarding claim 63, Christiansen teaches the method according to claim 62 wherein the layer to be strained (layer 50 in fig. 13) is locally strained in regions which are vertical in a plane with the defect region.

35. Regarding claim 64, Christiansen teaches the method according to claim 13 wherein the defect region is produced at a spacing of 50 to 500 nanometers from the layer to be relaxed. Several SiG layers having defects are to be relaxed. A spacing of the defects region of a SiGe layer is 300nm (the thickness of SiGe, paragraph [0018]) from the layer (a SiGe layer directly above or below) to be relaxed.

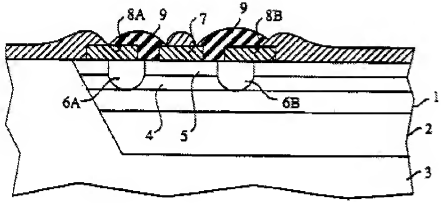
36. Regarding claim 66, Christiansen teaches the method according to claim 13, further comprising the step of removing the first and second layers (the sides of layer 400 in fig. 18, also layer 400 comprising several SiGe layer, see claim 26) after producing the strained layer or after producing a strained region.

37. Regarding claim 72, Christiansen teaches the method according to claim 1 wherein a strained layer or an unstrained layer are produced with a surface roughness of less than 1 nanometer (paragraph [0068]).

38. Claims 1, 4-5, 24, 48, 57, 67 are rejected under 35 U.S.C. 102(b) as being anticipated by Brasen et al (US Patent 5,442,205).

39. Regarding claim 1, Brasen teaches a method of producing a strained layer on a substrate, the method comprising the steps of: providing at least one first epitaxial relaxing layer (GeSi layer 5 in fig. 2) on an SOI-substrate, producing a defect region (layer 2) in a layer neighboring a silicon layer (layer 4) of the SOI-substrate to which strain is to be transferred, and relaxing (column 5) at least one layer neighboring the silicon layer to strain the silicon layer of the SOI-substrate and to produce the strained silicon layer.

FIG. 2



40. Regarding claim 4, Brasen teaches the method according to claim 1, further comprising the step of depositing the first layer (layer 5 in fig. 2) upon the silicon layer (layer 4) to be strained.

41. Regarding claim 5, Brasen teaches the method according to claim 4 wherein the first layer has a different degree of stress than the silicon layer to be strained (inherent due to different weights exerted on the layers).

42. Regarding claim 24, Brasen teaches the method according to claim 1 wherein the relaxation is carried out over a limited region of a layer (the top region, column 4, lines 14-19).

43. Regarding claim 48, Brasen teaches the method according to claim 1 Si-Ge (layer 5 in fig. 2) or Si-Ge-C or Si-C as the material for the first layer which is deposited on the layer to be strained.

44. Regarding claim 57, Brasen teaches the method according to claim 1 wherein the silicon layer (layer 4 in fig. 2) to be strained has a thickness d3 in the range of 5 to 30 nanometers (column 6, lines 37-39).

45. Regarding claim 67, Brasen teaches the method according to claim 1 wherein wet chemical material-selective etching is used (EDP etching, column 4).

46. Claims 1, 19, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Imai et al (US Patent 5,847,419).

47. Regarding claim 1, Imai teaches a method of producing a strained layer on a substrate, the method comprising the steps of: providing at least one first epitaxial relaxing layer (layer 15 in fig. 3D) on an SOI-substrate, producing a defect region (inherent due to lattice different) in a layer neighboring a silicon layer (layer 16 in fig. 3D) of the SOI-substrate to which strain is to be transferred, and relaxing (layer 15, see column 8, lines 42-45) at least one layer neighboring the silicon layer to strain the silicon layer of the SOI-substrate and to produce the strained silicon layer.

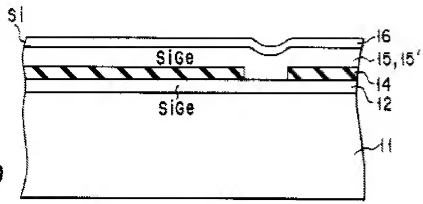


FIG. 3D

48. Regarding claim 19, Imai teaches the method according to claim 1, further comprising the step of relaxing the first layer by a thermal treatment (column 8, lines 42-45).

49. Regarding claim 22, Imai teaches a method according to claim 19 wherein the thermal treatment is carried out in an inert atmosphere (in nitrogen gas, see column 8, lines 42-45).

50. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

51. Claims 97-98 are rejected under 35 U.S.C. 102(e) as being anticipated by Usuda et al (US Patent 6,690,043 B1).

52. Regarding claim 97, Usuda teaches a method of producing a strained layer on a substrate, the method comprising the steps of: providing only one first relaxing layer (SeGe layer 4 in fig. 4B) on an SOI- substrate; producing a defect region (inherent due to lattice mismatch between Si layer 6 and SiGe layer 4) in the first layer; and relaxing the first layer and simultaneously straining a neighboring thin silicon layer of the SOI-substrate to produce the strained silicon layer (column 9, lines 26-34).

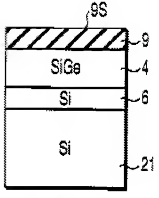


FIG. 4B

53. Regarding claim 98, Usuda teaches a method of producing a strained layer on a substrate, the method comprising the steps of: providing a first relaxing layer (layer 11 in fig. 11B) on an SOI-substrate; epitaxially forming a second layer (less than 10 nm thick Si layer 10, column 13, lines 42-45) with a different structure on the first layer; producing a defect region in the second layer; and relaxing the first layer and simultaneously straining a thin adjacent layer of the SOI-substrate to produce the strained silicon layer (column 9, lines 26-34).

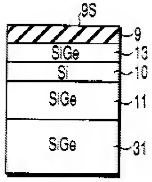


FIG. 11B

Claim Rejections - 35 USC § 103

54. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

55. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

56. Claims 58-59, 65, 68, and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brasen et al (US Patent 5,442,205) as applied to claims 57, 1, and 67 above, and further in view of Christiansen et al (PG Pub 2002/0185686 A1).

57. Regarding claim 58, Brasen remains as applied in claim 57. However, Brasen does not teach that the first layer has a thickness d4 close to a critical layer thickness for pseudomorphic growth. Christiansen teaches a layer having a thickness close to a critical layer thickness for pseudomorphic growth (layer 410 in fig. 13 having a thickness of 100nm, see paragraph [0085]). Also note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

58. Regarding claim 59, Christiansen teaches a layer thickness ratio d4/d3 (layer 410 to layer 50 in fig. 13) is greater than about 10.

59. Regarding claim 65, Christiansen teaches the defect region is at a spacing of 50 to l00 nanometers above the first layer on the layer to be strained (paragraph [0032]).

60. Regarding claim 68, Christiansen teaches the method according to claim 67, further comprising the step of etching trenches in the depth of the layers (paragraph [0008]).

61. Regarding claim 70, Brasen teaches the method according to claim 68, further comprising the step of filling the trenches with insulating material (layer above n+ layer 43 and between n layers 43 in fig. 4) to produce shallow trench insulation.

62. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen et al (PG Pub 2002/0185686 A1) as applied to claim 1 above, and further in view of Jerome et al (US Patent 5,344,785).

63. Regarding claim 43, Christiansen remains as applied in claim 1. However, Christiansen does not teach that an SIMOX or BESOI substrate is selected as a base structure for the substrate. In the same field of endeavor, Jerome teaches a BESOI substrate for the benefit of providing a substrate with lower defects. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a BESOI substrate for a base structure for the substrate for the benefit of providing a substrate with lower defects.

64. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen et al (PG Pub 2002/0185686 A1) as applied to claim 72 above, and further in view of Dhaka et al (US Patent 3,634,204).

65. Regarding claim 73, Christiansen remains as applied in claim 72. However, Christiansen does not teach that gate dielectric layer 102 is a thermal oxide layer. In the same field of endeavor, Dhaka teaches a dielectric layer being a thermal oxide (layer 12 in fig. 1B). Note that it would have been obvious to one of ordinary skill in that art at the time of the invention to have layer 102 of Christiansen's reduce the surface roughness (by filling layers into gaps caused by uneven surface) of the layer below to prevent layer 102 from pealing.

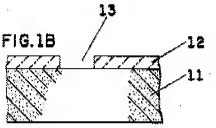


FIG.1B

66. Claims 67-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al (US Patent 5,847,419) as applied to claim 1 above, and further in view of Brasen et al (US Patent 5,442,205).

67. Regarding claim 67, Imai remains as applied in claim 1. However, Imai does not teach wet etching. Brasen teaches wet chemical material-selective etching is used (EDP etching, column 4). Note that there are only a limited techniques for etching and Brasen teaches wet chemical material-selective etching. "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007).

68. Regarding claim 68, Imai teaches the method according to claim 67, further comprising the step of etching trenches in the depth of the layers (layer 14 in fig. 3D).

69. Regarding claim 69, Imai teaches the method according to claim 68, further comprising the step, after producing the etched trenches (in layer 14 in fig. 3D), of relaxing the first layer or a further layer by a thermal treatment (column 8, lines 29-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FYL

/Feifei Yeung-Lopez/
Examiner, Art Unit 2826

/Leonardo Andújar/
Primary Examiner, Art Unit 2826